

• General Description

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. It combines one N channel MOSFET and one P channel MOSFET

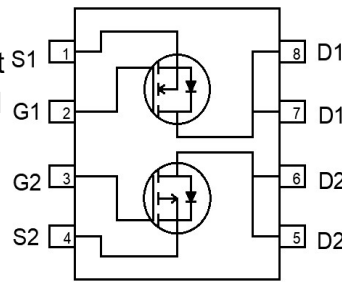
• Features

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Dual DIE in one package
- Low Thermal resistance

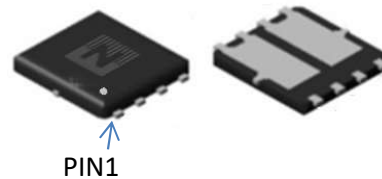
• Application

- BLDC Motor driver
- Load switch

• Product Summary



$V_{DS1} = 40V$
 $V_{DS2} = -40V$
 $R_{DS(ON)1} = 18m\Omega$
 $R_{DS(ON)2} = 45m\Omega$
 $I_{D1} = 23A$
 $I_{D2} = -14A$



DFN3*3



• Ordering Information:

Part NO.	ZMCA88405M
Marking	C88405
Packing Information	REEL TAPE
Basic ordering unit (pcs)	5000

• N Channel Absolute Maximum Ratings ($T_C=25^\circ C$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		40	V
Gate-Source Voltage ^①	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ C$	23	A
	I_D	$T_C=75^\circ C$	19	A
	I_D	$T_C=100^\circ C$	16	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25^\circ C$;	69	A
Total Power Dissipation	P_D	$T_C=25^\circ C$	26	W
Total Power Dissipation	P_D	$T_A=25^\circ C$	2.5	W
Operating Junction Temperature	T_J		-55 to +175	$^\circ C$
Storage Temperature	T_{STG}		-55 to +175	$^\circ C$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1mH, V_{GS}=10V, R_g=25\Omega,$	14	mJ
		$L=0.5mH, V_{GS}=10V, R_g=25\Omega,$	29.4	mJ
ESD Level (HBM)	CLASS 1B			

•P Channel Absolute Maximum Ratings (T_C=25°C)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V _{DS}		-40	V
Gate-Source Voltage ^②	V _{GS}		±20	V
Continuous Drain Current	I _D	T _C =25°C	-14	A
	I _D	T _C =75°C	-12	A
	I _D	T _C =100°C	-10	A
Pulsed Drain Current	I _{DM}	Pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C;	-42	A
Total Power Dissipation	P _D	T _C =25°C	26	W
Total Power Dissipation	P _D	T _A =25°C	2.5	W
Operating Junction Temperature	T _J		-55 to +175	°C
Storage Temperature	T _{STG}		-55 to +175	°C
Single Pulse Avalanche Energy	E _{AS}	L=0.1mH, V _{GS} =-10V, R _g =25Ω,	15	mJ
		L=0.5mH, V _{GS} =-10V, R _g =25Ω,	27	mJ
ESD Level (HBM)	CLASS 2			

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R _{thJC}		-	5.8	°C/W
Thermal resistance, junction-ambient ^③	R _{thJA}		-	60	°C/W
Soldering temperature	T _{sold}		-	260	°C

•N Channel Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.3	1.7	2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=40V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=8A$		18	23	m Ω
		$V_{GS}=4.5V, I_D=6A$		26	35	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_{SD}=2A$		1.8		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=8A$			1.3	V

•N Channel Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=25V$	-	805	-	pF
Output capacitance	C_{oss}		-	94	-	
Reverse transfer capacitance	C_{rss}		-	58	-	
Gate Resistance	R_g	$f=1MHz$	-	1.4		Ω
Total gate charge	Q_g	$V_{DD}=15V, I_D=10A, V_{GS}=10V$	-	12	-	nC
	$Q_g(4.5v)$		-	6.5	-	
Gate - Source charge	Q_{gs}		-	2.8	-	
Gate - Drain charge	Q_{gd}		-	3.1	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=10A$	-	9	-	ns
Turn-ON Rise time	t_r		-	2	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	10	-	ns
Turn-Off Fall time	t_f		-	8	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=20V, di_s/dt=100A/\mu s, I_S=10A$	-	32	-	ns
Reverse Recovery Charge	Q_{RR}		-	25	-	nC

•P Channel Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.3	-1.7	-2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-40V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-6A$		45	60	m Ω
		$V_{GS}=-4.5V, I_D=-5A$		55	80	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_{SD}=-2A$		1.2		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=-6A$			1.3	V

•P Channel Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=-25V$	-	838	-	pF
Output capacitance	C_{oss}		-	94	-	
Reverse transfer capacitance	C_{rss}		-	70	-	
Gate Resistance	R_g	$f=1MHz$	-	9.2		Ω
Total gate charge	Q_g	$V_{DD}=-15V, I_D=-10A, V_{GS}=-10V$	-	15.3	-	nC
	$Q_g(4.5V)$		-	7.5	-	
Gate - Source charge	Q_{gs}		-	3.6	-	
Gate - Drain charge	Q_{gd}		-	2.3	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=-10V, V_{DS}=-15V, R_G=3.3\Omega, I_D=-10A$	-	20	-	ns
Turn-ON Rise time	t_r		-	174	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	43	-	ns
Turn-Off Fall time	t_f		-	10.4	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=-20V, dI_S/dt=100A/\mu s, I_S=-10A$	-	58	-	ns
Reverse Recovery Charge	Q_{RR}		-	75	-	nC

• N Channel characteristics curve

Fig.1 Gate-Charge Characteristics

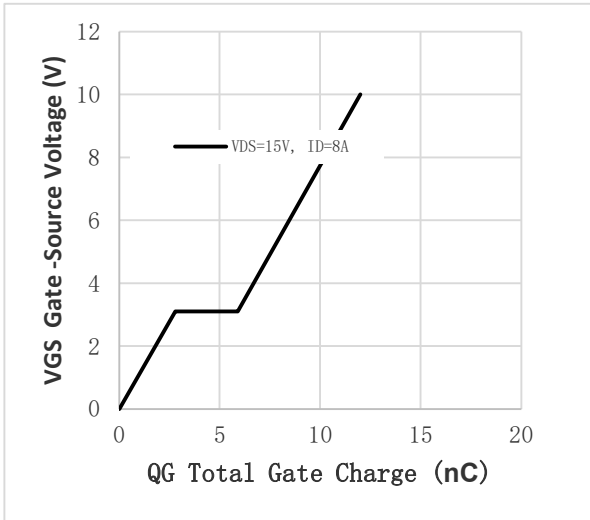


Fig.2 Capacitance Characteristics

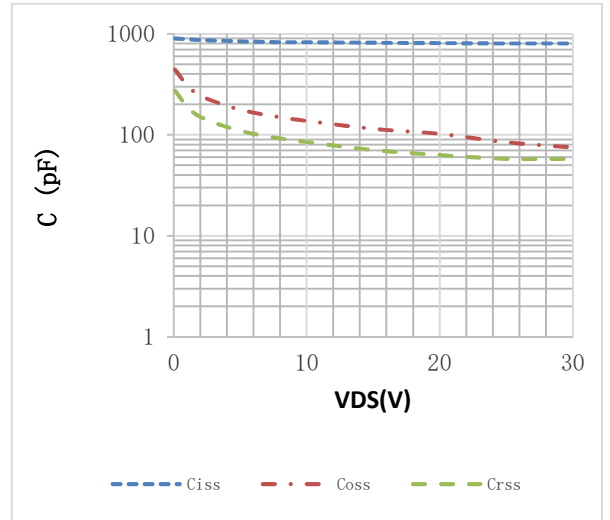


Fig.3 Power Dissipation

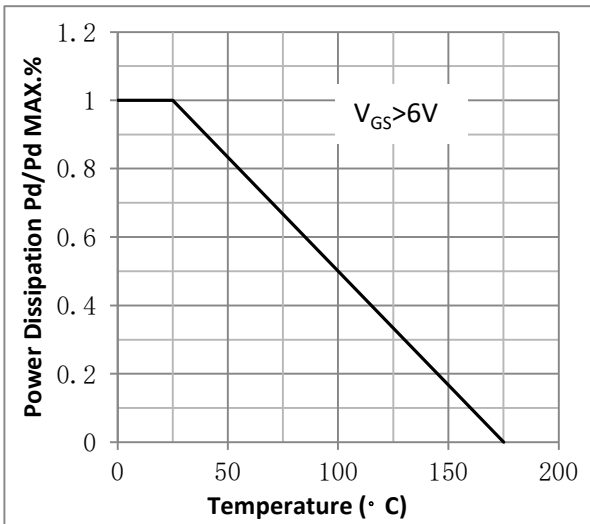


Fig.4 Typical output Characteristics

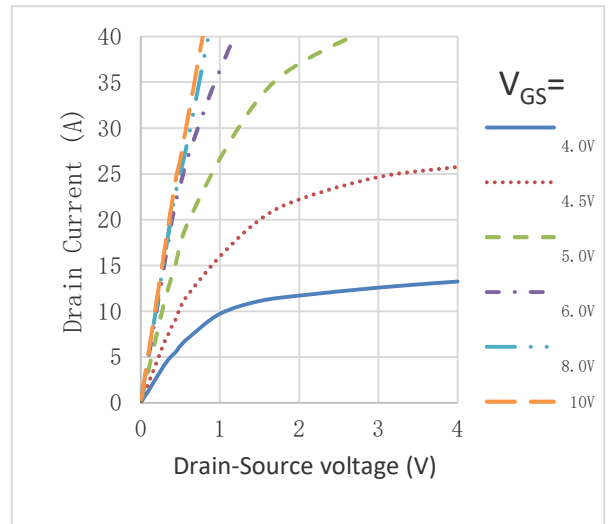


Fig.5 Threshold Voltage V.S Junction Temperature

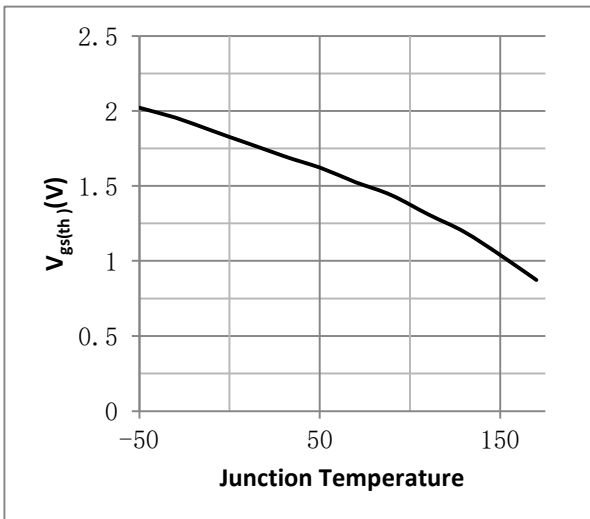


Fig.6 Resistance V.S Drain Current

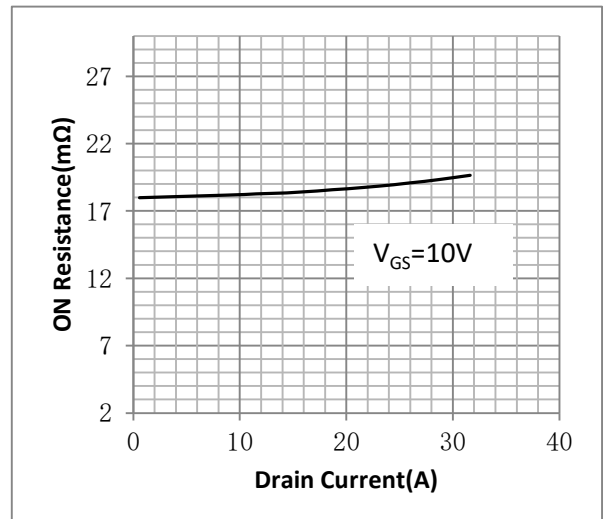


Fig.7 On-Resistance VS Gate Source Voltage

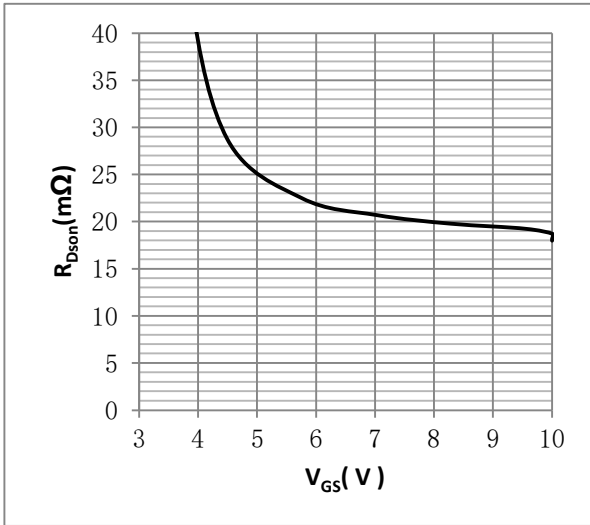


Fig.8 On-Resistance V.S Junction Temperature

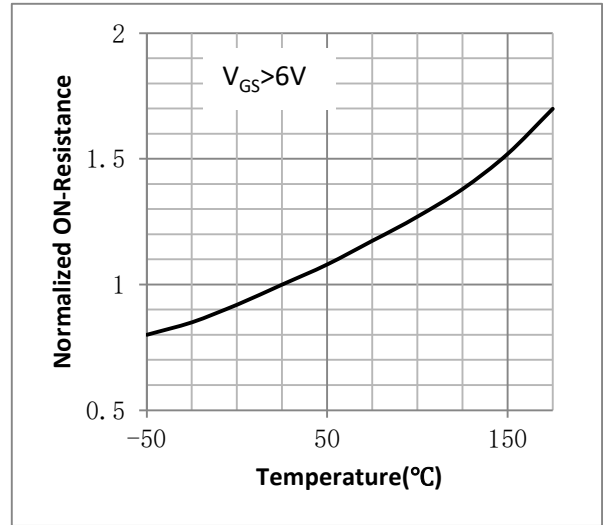


Figure 9. Diode Forward Voltage vs. Current

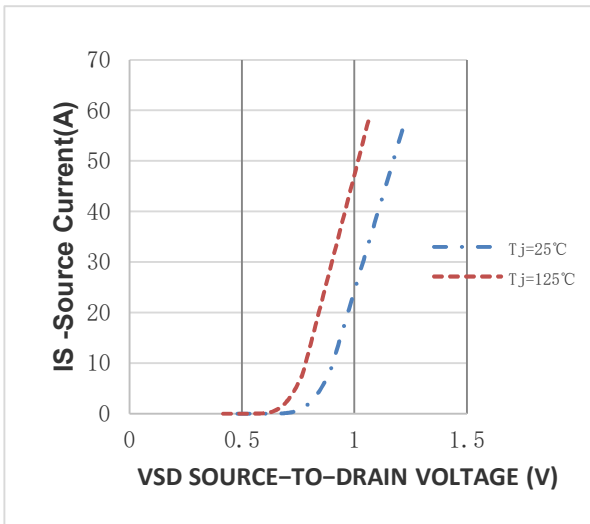


Figure 10. Transfer Characteristics

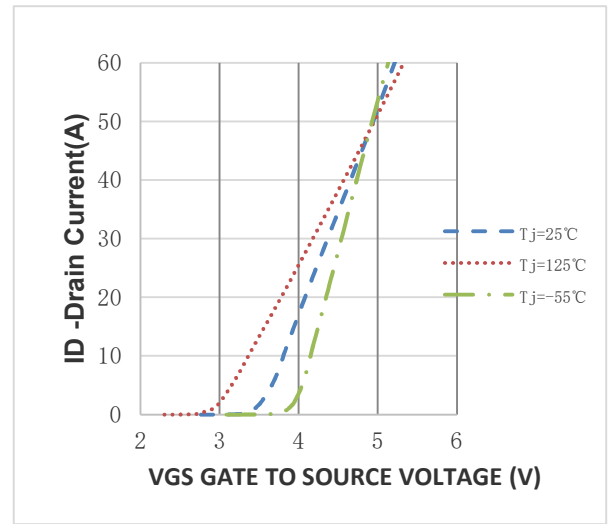


Fig.11 Safe Operating Area

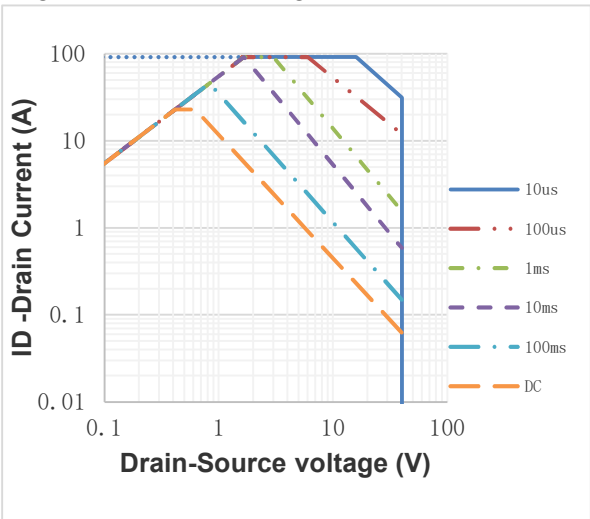
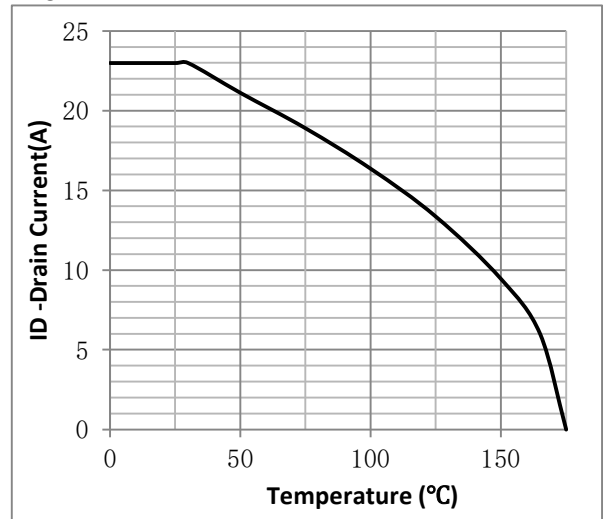


Fig.12 ID vs. Case Temperature^④



• Channel characteristics curve

Fig.1 Gate-Charge Characteristics

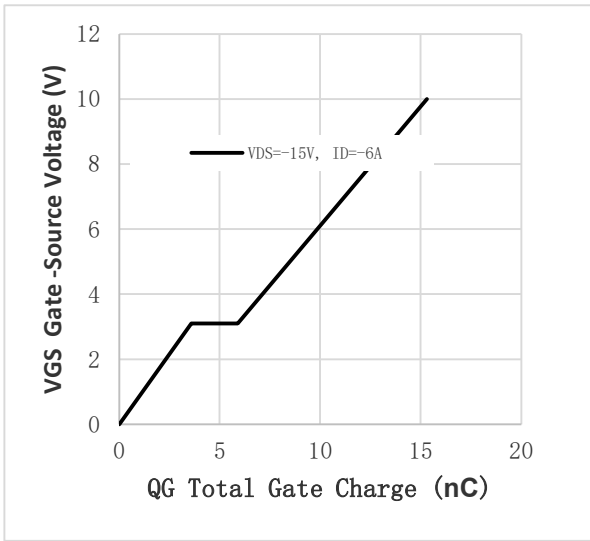


Fig.2 Capacitance Characteristics

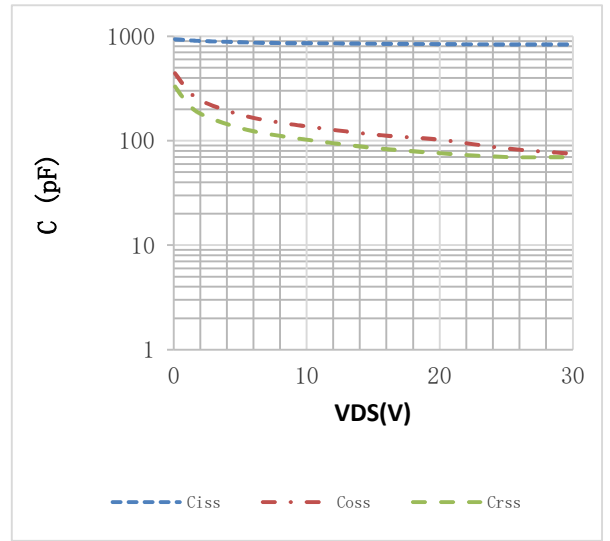


Fig.3 Power Dissipation

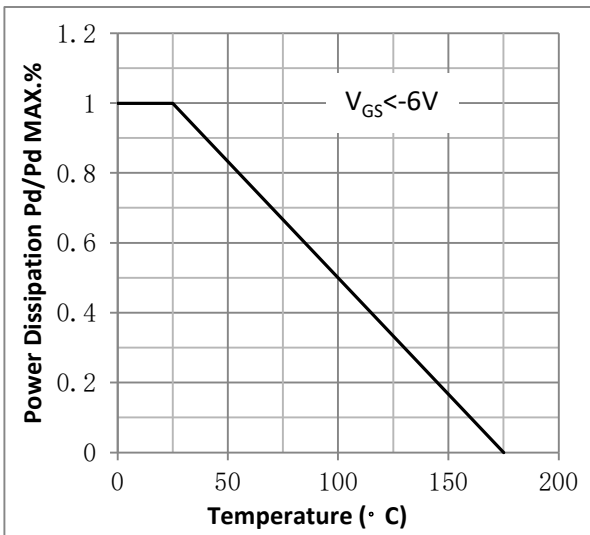


Fig.4 Typical output Characteristics

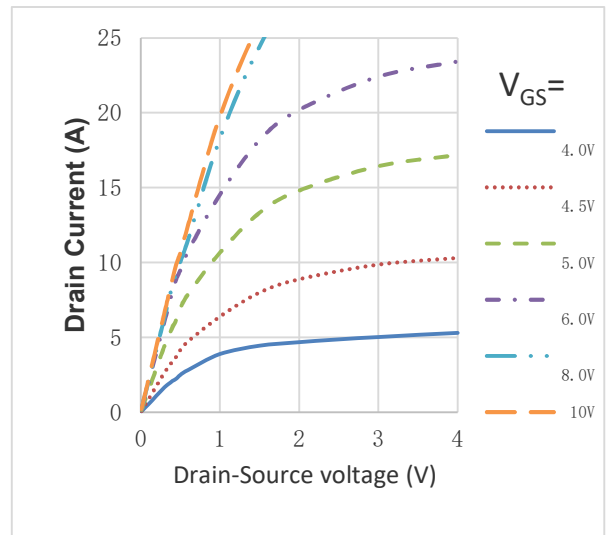


Fig.5 Threshold Voltage V.S Junction Temperature

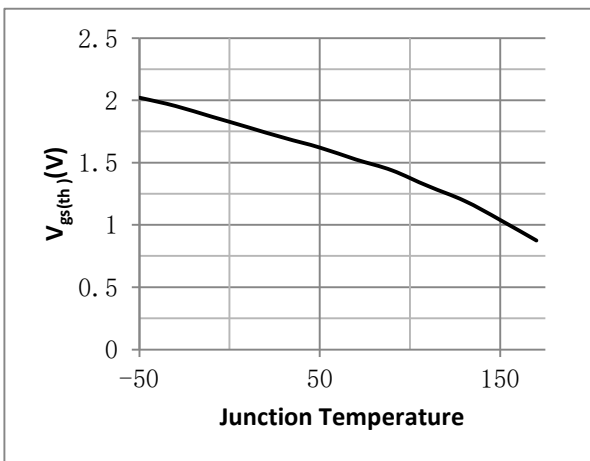


Fig.6 Resistance V.S Drain Current

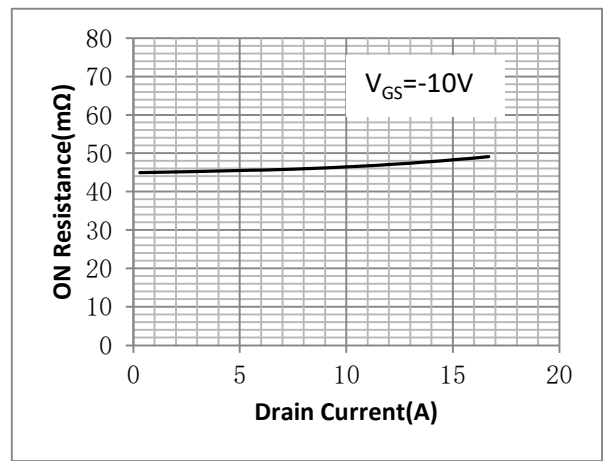


Fig.7 On-Resistance VS Gate Source Voltage

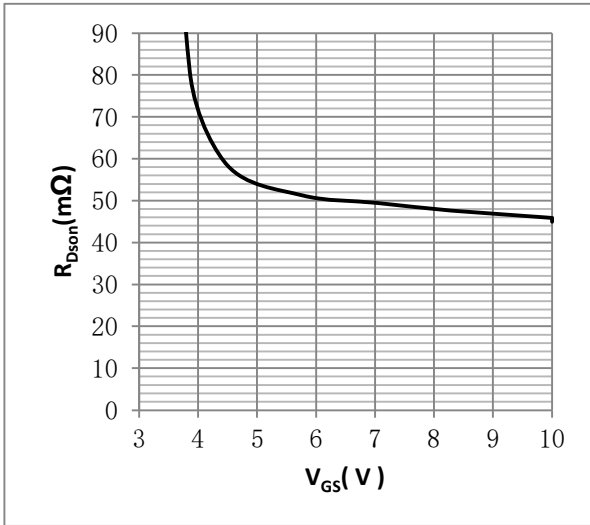


Fig.8 On-Resistance V.S Junction Temperature

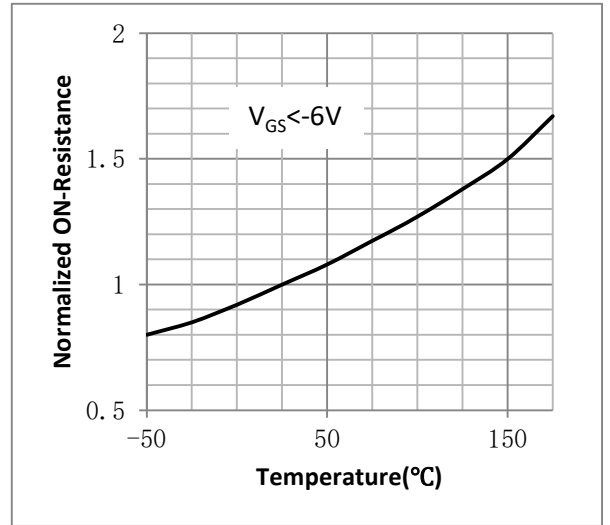


Figure 9. Diode Forward Voltage vs. Current

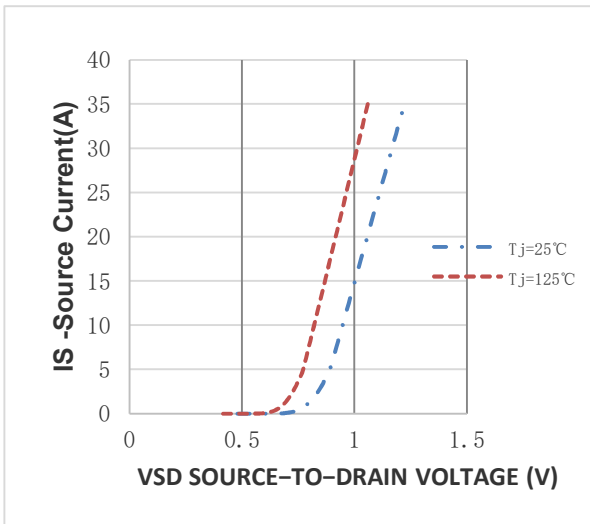


Figure 10. Transfer Characteristics

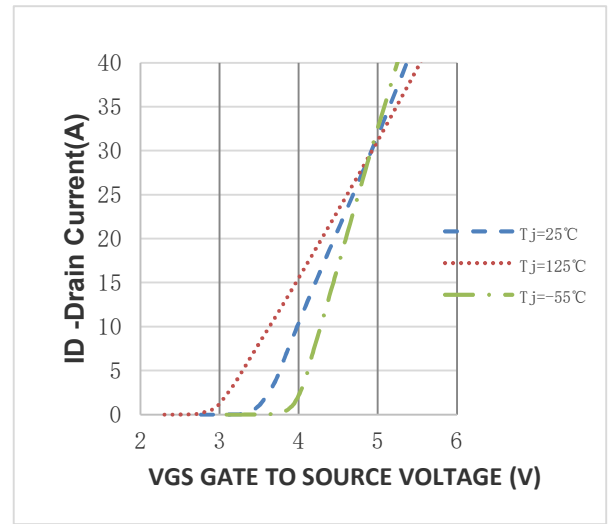


Fig.11 Safe Operating Area

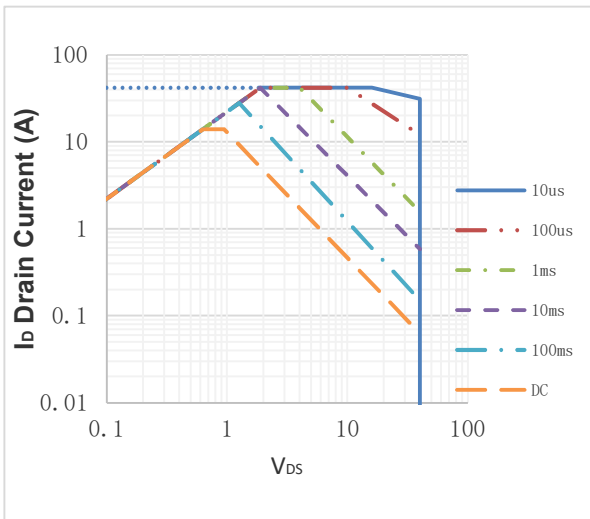
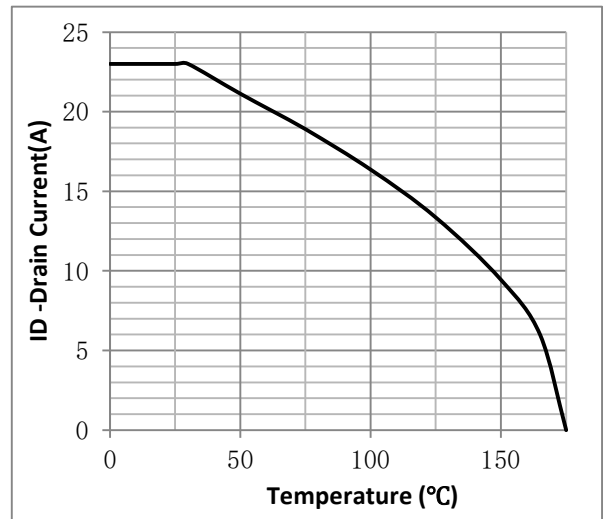
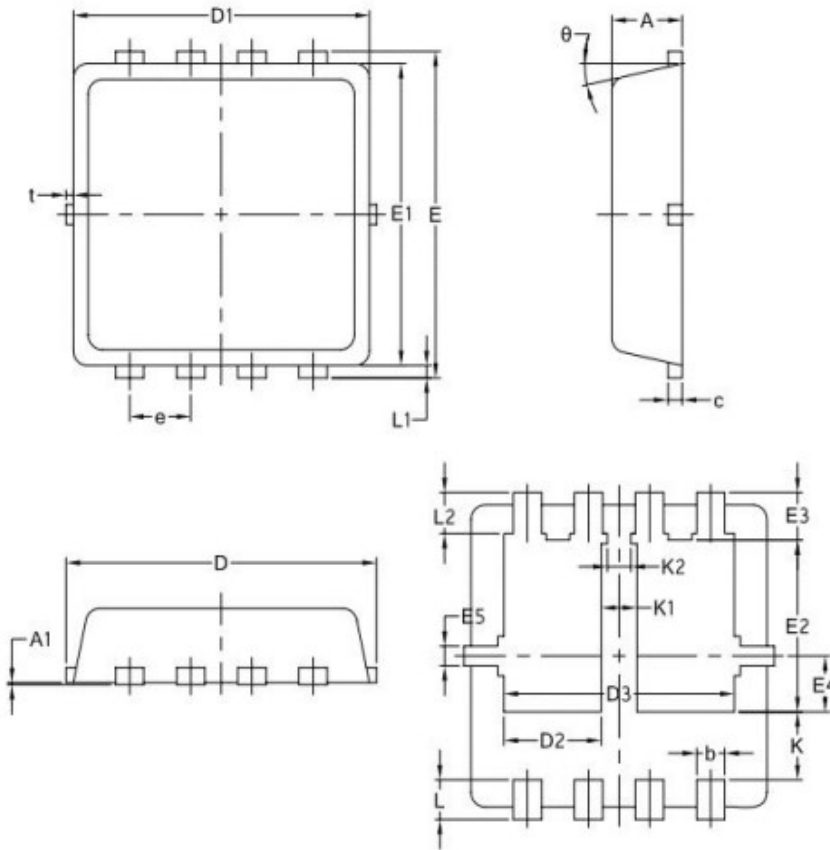


Fig.12 ID vs. Case Temperature^④



•DFN3*3 Package Outline



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.25	0.30	0.39
c	0.14	0.152	0.20
D	3.20	3.30	3.45
D1	3.05	3.15	3.25
D2	0.84	1.04	1.24
D3	2.30	2.45	2.60
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.60	1.74	1.90
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.50	0.69	0.80
K1	0.30	0.38	0.53
K2	0.15	0.25	0.35
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
L2	0.27	0.42	0.57
t	0	0.075	0.13
θ	10°	12°	14°

Note:

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours ;
- ② Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=-20V/+10V$, $T_j=175^{\circ}C$, $t=1000$ hours ;
- ③ Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ④ Practically the current will be limited by PCB, thermal design and operating temperature.
 $V_{GS}=10V$ (N channel)/-10V(P channel).

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- Since ZMJ uses lot number as the tracking base, please provide the lot number for tracking when complaining.

Revision History

Version	Date	Change
A	2023.3.16	NEW
B	2023.11.3	Correct Package outline and Circuit diagram
C	2023.11.30	Correct marking